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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/763,643 | 01/23/2004 | Yu Min Lin | 24061.69 (TSMC2002-1055/1 | 7730 |

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| EXAMINER | |
|---|---|
| SARKAR, ASOK K | |
| **ART UNIT** | **PAPER NUMBER** |
| 2891 | |

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,643 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Asok K. Sarkar | 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *56-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of Gp I claims 1 – 55 in the reply filed on June 27, 2005 is acknowledged. The traversal is on the ground(s) that the embodiments delineated by the Examiner are not patentably distinct and therefore constitute a single invention concept. This is not found persuasive because these inventions are distinct for the reasons given in the restriction requirement mailed May 23, 2005 and has acquired a separate status in the art as shown by their different classification. Moreover, search criteria for the two classes are different.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 56 – 60 were withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group II claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on June 27, 2005.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 13 – 15 and 19 – 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Pomarede, US 2002/0098627.

Regarding claims 13 and 14, Pomarede teaches a method for fabricating a

portion of an integrated circuit on a semiconductor substrate, the method comprising:

- placing a pseudo-substrate of silicon (paragraph 61)in a process reactor in step 120 of Fig. 3;
- applying a loading treatment to the pseudo-substrate in step 125 of Fig. 3 (paragraph 84);
- removing the pseudo-substrate from the process reactor;
- placing a device substrate into the process reactor (paragraph 86); and
- forming a poly-silicon layer upon the device substrate in step 130 of Fig. 3 (paragraph 86) with descriptions in paragraphs describing the process flow in paragraph 60 that covers paragraphs 61 – 103.

Regarding claim 15, Pomarede teaches selecting a first temperature, a first pressure, and a first time for the loading treatment; and selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation in paragraphs 65 and 86.

Regarding claims 19 and 20, Pomarede teaches selecting a chemical such as $NH_3$ for the loading treatment in paragraph 66.

Regarding claims 21 and 22, Pomarede teaches performing the loading treatment within the same process environment as the polysilicon formation or within an individual process environment in paragraph 86.

Regarding claim 23, Pomarede teaches employing plasma for the loading treatment in paragraph 66.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 16 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomarede, US 2002/0098627.

Regarding these claims Pomarede teaches using the first temperature between

550 – 750°C and a pressure between 0.1 – 80 Torr in paragraph 65 and using the second temperature between 700 – 900°C and a pressure between I millitorr – 760 Torr in paragraphs 94 and 95.

Pomarede fails to teach the time parameter for these two treatments.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the time parametrs during the loading treatment and the gate electrode deposition treatment through routine experimentation and optimization to achieve optimum benefits especially there is a limited thickness for the gate as disclosed by Pomarede (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

9. Claims 42, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975.

Regarding claim 42, Colombo teaches a method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

- forming a thin insulate 106 on the substrate 104 (see Fig. 2A);
- depositing a high dielectric constant (high-k) material 110 upon the thin insulate;

- performing an anneal on the high-k material (step 10 in Fig. 1);
- applying a loading treatment (step 8 in Fig. 1)upon the high-k material; and
- forming a poly-silicon layer (step 14 in Fig. 1) on the treated high-k material, wherein the anneal and poly-silicon deposition occur sequentially (see Fig. 1) as discussed in between column 6, line 7 and column 8, line 25.

Colombo fails to teach cleaning the surface of the substrate.

Ahn teaches cleaning of the substrate for the benefit of minimizing the oxide at the interface for forming high dielectric constant metal oxide gate dielectric in paragraph 24.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo and clean the surface of the substrate for the benefit of minimizing the oxide at the interface for forming high dielectric constant metal oxide gate dielectric as taught by Ahn in paragraph 24.

Regarding claim 51, Colombo teaches loading treatment employing plasma in step 8 of Fig. 1.

Regarding claim 52, Colombo teaches depositing high – k material by ALD process in column 5, line 31.

10. Claims 43 – 50, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975 as applied to claim 42 above, and further in view of Pomarede, US 2002/0098627.

Regarding claims 43 – 50, Colombo in view of Ahn fails to teach the limitations.

Pomarede teaches these limitations as were described earlier in rejecting claims 13 – 22.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo in view of Ahn and further in view of Pomarede for the benefit of applying these processing parameters of these claims as were described earlier in rejecting claims 13 – 22.

Regarding claims 53 and 54, Colombo in view of Ahn teaches the ALD process for $HfO_2$, but fails to teach the deposition processing parameters.

Pomarede teaches the temperature range of between 200 – 400$^{o}$C for the ALD process and cycling of the deposition process and the deposition depth of 3 – 75 Angstroms in paragraphs 80 – 83 for the benefit of improving speed, efficiency, quality and uniformity of the depositing layers in paragraph 17.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo in view of Ahn and apply the processing parameters and depth of the deposited layer of $HfO_2$ for the benefit of improving speed, efficiency, quality and uniformity of the depositing layers as taught by Pomarede in paragraph 17.

11. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975 as applied to claim 42 above, and further in view of Rayssac, US 2004/0178448.

Colombo in view of Ahn fails to teach diamond substrate.

Rayssac teaches the use of diamond substrate with high – k gate dielectrics for

the benefit of providing a high thermal conductivity in paragraph 9.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo in view of Ahn any use a diamond substrate for the benefit of providing a high thermal conductivity as taught by Rayssac in paragraph 9.

12. Claims 1, 9, 24 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975; Rotonadaro, 2002/0081826 and Rotonadaro, 2005/0124121.

Regarding claims 1 and 24, Colombo teaches a method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

- forming a thin insulate 106 on the substrate 104 (see Fig. 2A);
- depositing a high dielectric constant (high-k) material 110 upon the thin insulate;
- performing an anneal on the high-k material (step 10 in Fig. 1) in two steps one is a non – oxidizing anneal and the other is an oxygen – based anneal wherein both anneals occur sequentially in column 7, lines 1 – 25;
- applying a loading treatment (step 8 in Fig. 1)upon the high-k material; and
- forming a poly-silicon layer (step 14 in Fig. 1) on the treated high-k material, wherein the loading treatment and poly-silicon deposition occur sequentially (see Fig. 1) as discussed in between column 6, line 7 and column 8, line 25.

Colombo fails to teach (1) cleaning the surface of the substrate, and (2) performing a hydrogen – based anneal on the high – k material.

Regarding element (1), Ahn teaches cleaning of the substrate for the benefit of

minimizing the oxide at the interface for forming high dielectric constant metal oxide gate dielectric in paragraph 24.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo and clean the surface of the substrate for the benefit of minimizing the oxide at the interface for forming high dielectric constant metal oxide gate dielectric as taught by Ahn in paragraph 24.

Regardinr element (2), Rotonadaro teaches that a hydrogen – based anneal on the high – k material is good for the benefit of annealing or defect passivation in gate dielectric layer in paragraph 20 (2002) and in paragraph 40 (2005).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo and apply a hydrogen – based anneal on the high – k material for the benefit of annealing or defect passivation in gate dielectric layer as taught by Rotonadaro in paragraph 20 (2002) and in paragraph 40 (2005).

Regarding claims 9 and 35, Colombo teaches depositing high – k material by ALD process in column 5, line 31.

13. Claims 2 – 8, 10, 11, 25 – 34 and 36 – 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975; Rotonadaro, 2002/0081826 and Rotonadaro, 2005/0124121 as applied to claims 1 and 24 above, and further in view of Pomarede, US 2002/0098627.

Regarding claims 2, 25 and 29 – 31, Colombo teaches, pressure and time for the first and second temperatures in column 7, lines 1 – 25, but fails to teach the, pressure and time for the third and fourth temperatures.

Pomarede teaches the temperature range and the pressure ranges for the loading and the polysilicon deposition as was described earlier in rejecting claims 16 – 18 for the benefit of improving speed, efficiency, quality and uniformity of the depositing layers in paragraph 17.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Colombo and select the processing parameters for the loading and the polysilicon deposition for the benefit of improving speed, efficiency, quality and uniformity of the depositing layers as taught by Pomarede in paragraph 17.

Regarding claims 3 – 5 and 26 – 28, Colombo teaches the processing parameters such as pressure, temperature and time for these claims in column 7, lines 1 – 25.

Regarding claims 6 – 8 and 32 – 34, Rotonadaro teaches the chemicals for the hydrogen – based anneal as $H_2$ or $NH_3$ in layer in paragraph 20 (2002) and in paragraph 40 (2005); Colombo teaches the second chemical for the oxygen – based anneal as $O_2$, $N_2O$ and NO in column 7, lines 1 – 25 and third chemical in column 6, lines 28 – 35 and these chemicals are dependent on the particular high –k material chosen as taught by Colombo.

Regarding claims 10, 11 and 36 – 40, limitations of these claims have been described earlier in rejecting claims 21 – 23 and claims 51 – 53.

14. Claims 12 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo, US 6,809,370 in view of Ahn, US 2002/0192975; Rotonadaro,

2002/0081826 and Rotonadaro, 2005/0124121 as applied to claims 1 and 24 above, and further in view of Rayssac, US 2004/0178448.

Limitations of these claims have been described earlier in rejecting claim 55.

***Conclusion***

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
July 18, 2005

Primary Examiner